



US007924608B2

(12) **United States Patent**  
**Campbell**

(10) **Patent No.:** **US 7,924,608 B2**  
(45) **Date of Patent:** **Apr. 12, 2011**

(54) **FORCED ION MIGRATION FOR  
CHALCOGENIDE PHASE CHANGE  
MEMORY DEVICE**

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(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 364 days.

(21) Appl. No.: **11/875,805**

(22) Filed: **Oct. 19, 2007**

(65) **Prior Publication Data**

US 2008/0121859 A1 May 29, 2008

**Related U.S. Application Data**

(60) Provisional application No. 60/853,068, filed on Oct. 19, 2006.

(51) **Int. Cl.**  
**G11C 11/00** (2006.01)

(52) **U.S. Cl.** ..... **365/163**; 365/148; 257/2; 257/5;  
438/95; 977/754

(58) **Field of Classification Search** ..... 365/46,  
365/94, 100, 113, 129, 148, 163; 257/2-5,  
257/296, E31.047, E27.006; 438/29, 95,  
438/96, 166, 259, 365, 482, 486, 597; 977/754  
See application file for complete search history.

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*Primary Examiner* — Richard Elms

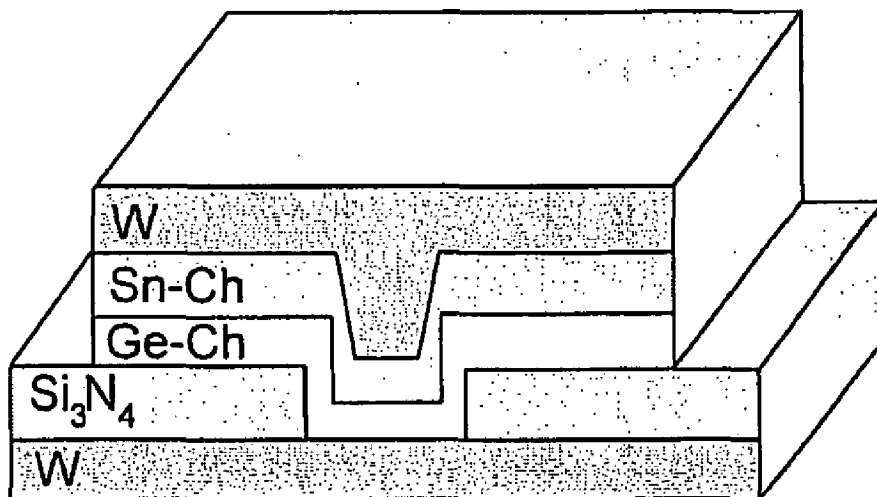
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(57) **ABSTRACT**

Non-volatile memory devices with two stacked layers of chalcogenide materials comprising the active memory device have been investigated for their potential as phase change memories. The devices tested included GeTe/SnTe, Ge<sub>2</sub>Se<sub>3</sub>/SnTe, and Ge<sub>2</sub>Se<sub>3</sub>/SnSe stacks. All devices exhibited resistance switching behavior. The polarity of the applied voltage with respect to the SnTe or SnSe layer was critical to the memory switching properties, due to the electric field induced movement of either Sn or Te into the Ge-chalcogenide layer. One embodiment of the invention is a device comprising a stack of chalcogenide-containing layers which exhibit phase change switching only after a reverse polarity voltage potential is applied across the stack causing ion movement into an adjacent layer and thus "activating" the device to act as a phase change random access memory device or a reconfigurable electronics device when the applied voltage potential is returned to the normal polarity. Another embodiment of the invention is a device that is capable of exhibiting more than two data states.

**20 Claims, 12 Drawing Sheets**



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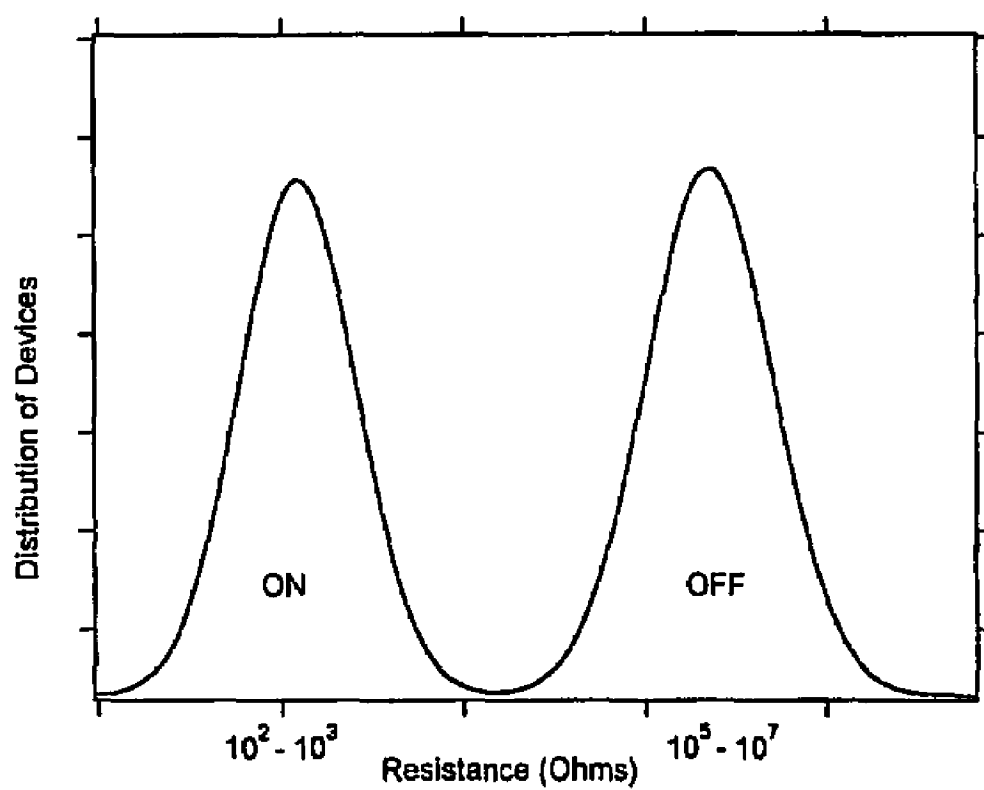


Fig. 1

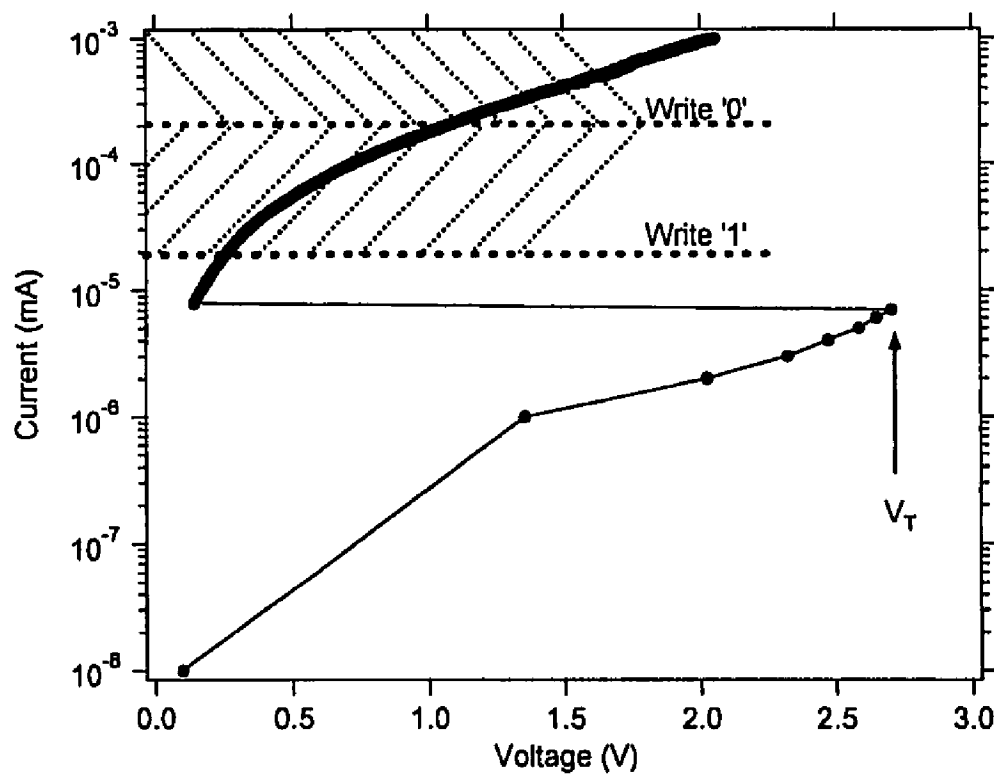


Fig. 2

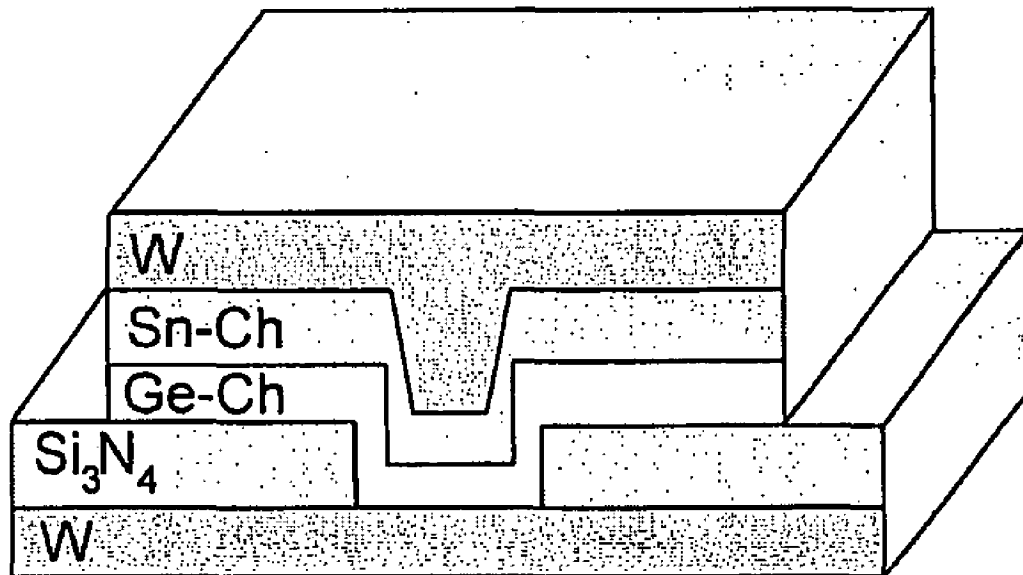


Fig. 3

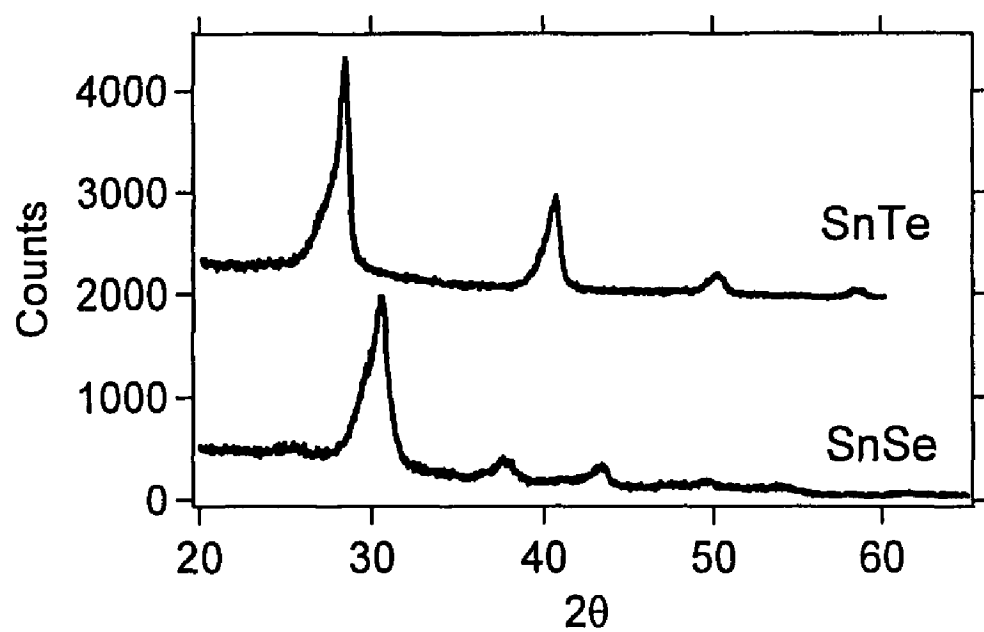
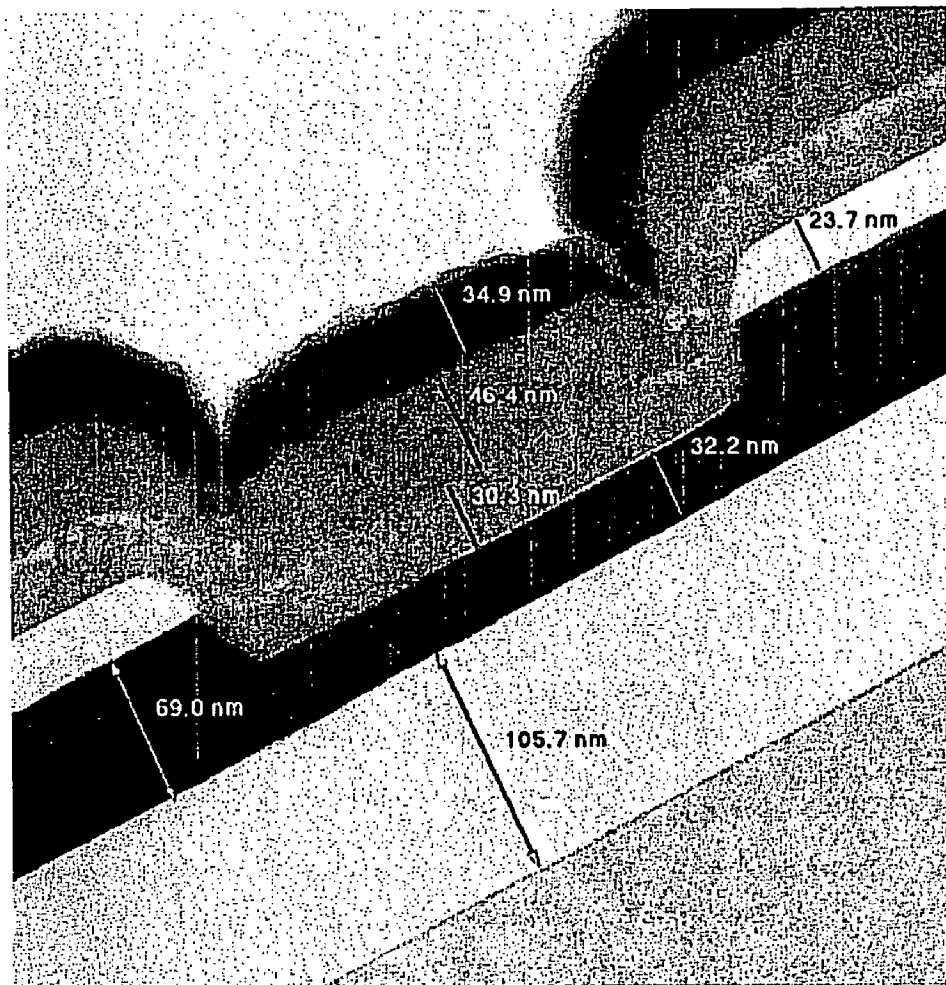


Fig. 4.



70.0 nm

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Any row 2, Pad 11,12

Fig. 5.



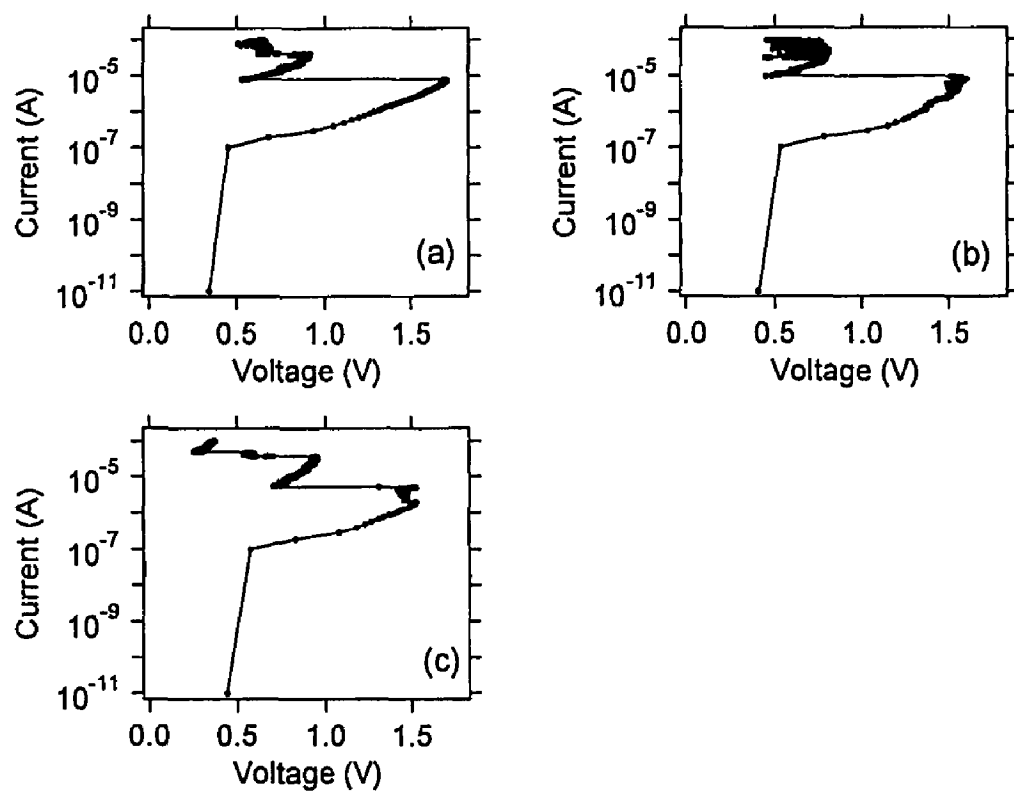


Fig. 6.

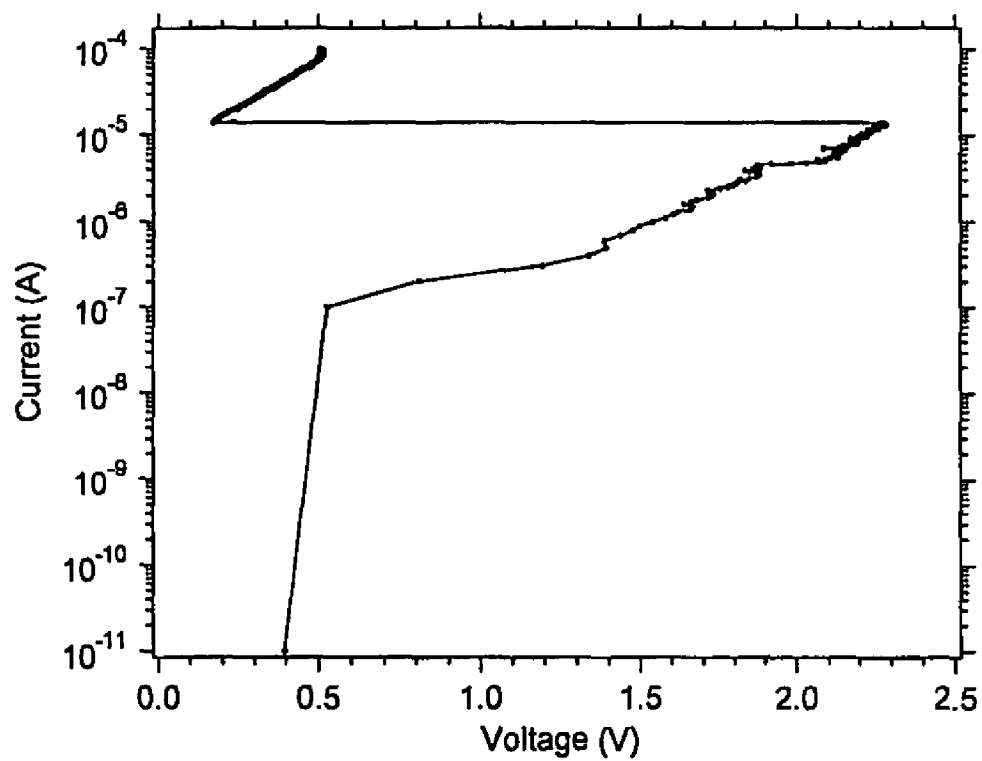


Fig. 7.

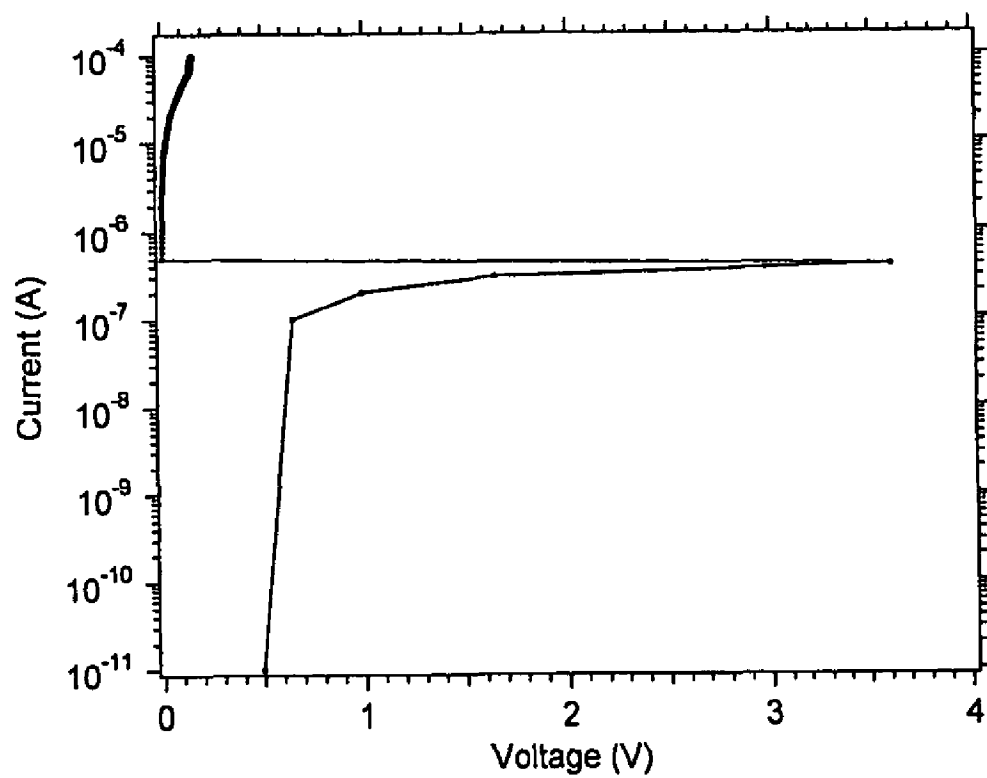


Fig. 8.

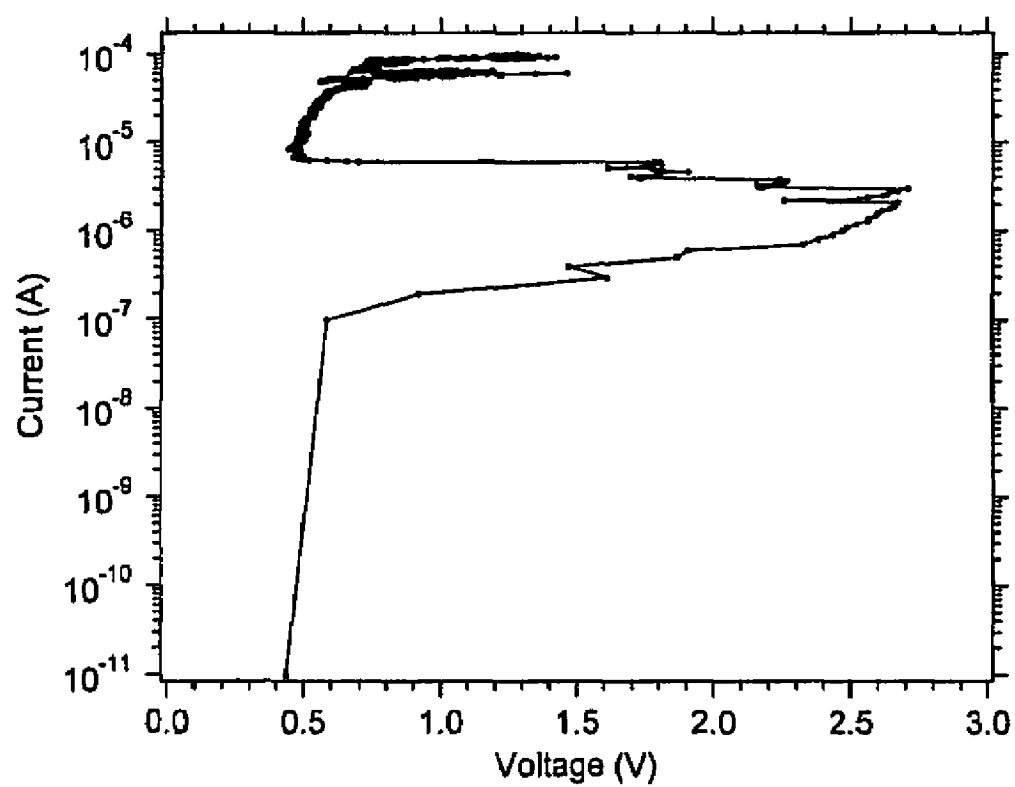


Fig. 9

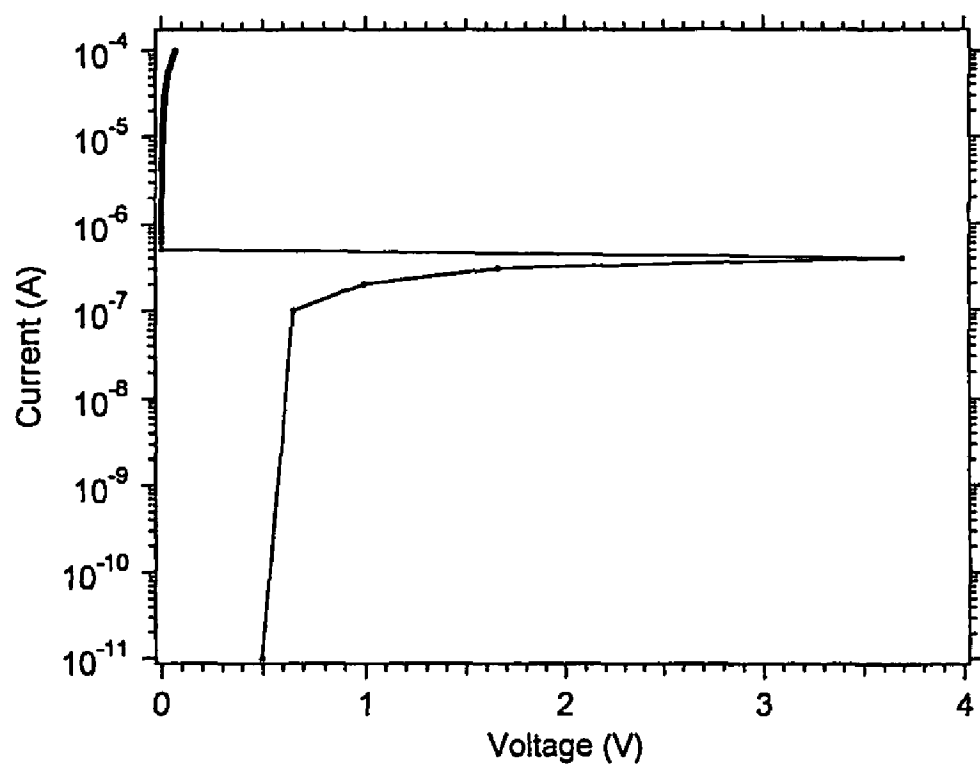


Fig. 10

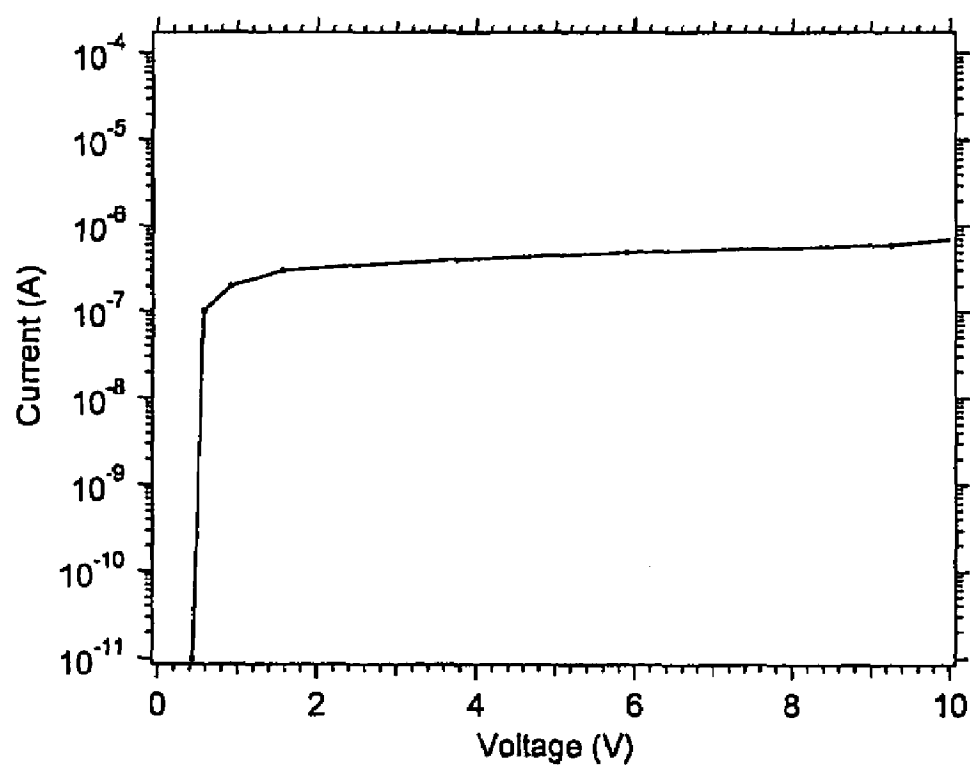


Fig. 11.

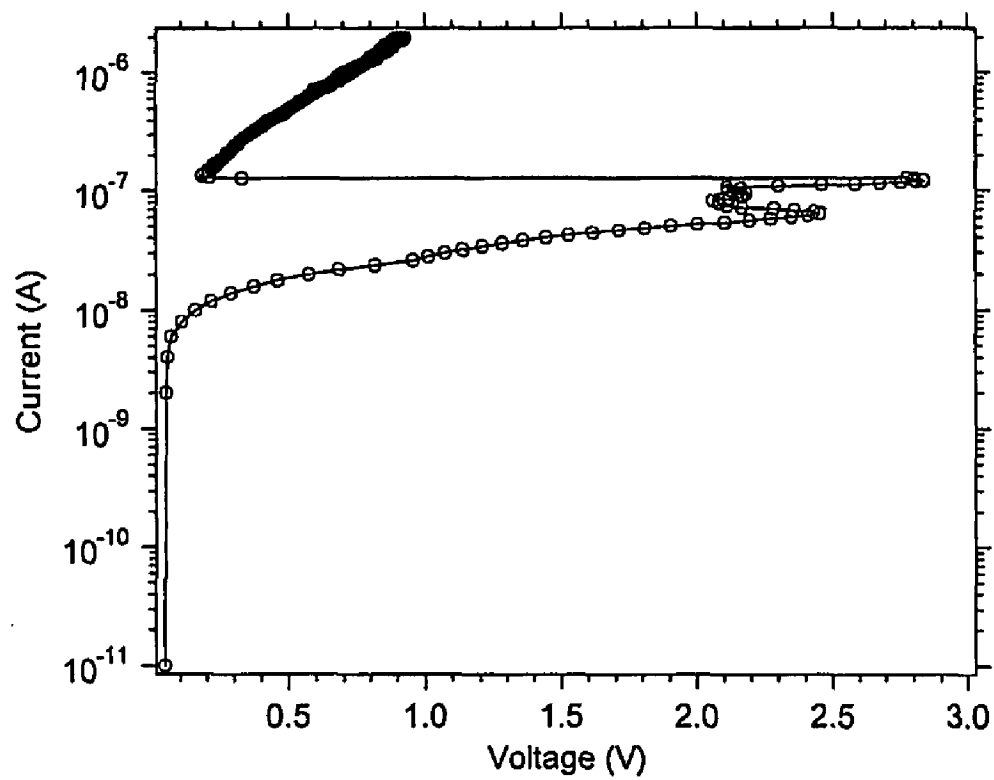


Fig. 12.

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# FORCED ION MIGRATION FOR CHALCOGENIDE PHASE CHANGE MEMORY DEVICE

This application claims priority of my prior provisional patent application, Ser. 60/853,068, filed on Oct. 19, 2006, entitled "Forced Ion Migration for Chalcogenide Phase Change Memory Device," which is incorporated herein by reference.

This work was partially supported by a NASA Idaho EPS-CoR grant, NASA grant NCC5-577.

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

This invention relates generally to electronic memory devices, and more particularly to a method of inducing a non-phase change stack structure into a phase change stack memory structure.

### 2. Related Art

Research into new random access electronic memory technologies has grown significantly in the past 10 years due to the near realization of the scaling limits of DRAM and the low cycle lifetime, high power requirements, and radiation sensitivity of Flash. At the forefront of this research is the phase-change random access memory (PCRAM) [see Bez, R.; Pirovano, A. "Non-volatile memory technologies: emerging concepts and new materials" *Materials Science in Semiconductor Processing* 7 (2004) 349-355; and Lacaita, A. L. "Phase-change memories: state-of-the-art, challenges and perspectives" *Solid-State Electronics* 50 (2006) 24-31]. Phase-change memory is a non-volatile, resistance variable memory technology whereby the state of the memory bit is defined by the memory material's resistance. Typically, in a two state device, a high resistance defines a logic '0' (or 'OFF' state) and corresponds to an amorphous phase of the material. The logic '1' ('ON' state) corresponds to the low resistance of a crystalline phase of the material. The 'high' and 'low' resistances actually correspond to non-overlapping resistance distributions, rather than single, well-defined resistance values (FIG. 1).

The phase-change material is switched from high resistance to a low resistance state when a voltage higher than a 'threshold' voltage,  $V_p$ , is applied to the amorphous material [see Adler, D.; Henisch, H. K.; Mott, N. "The Mechanism of Threshold Switching in Amorphous Alloys" *Reviews of Modern Physics* 50 (1978) 209-220; and Adler, D. "Switching Phenomena in Thin Films" *J. Vac. Sci. Technol.* 10 (1973) 728-738] causing the resistance to significantly decrease (FIG. 2). The resultant increased current flow causes Joule heating of the material to a temperature above the material glass transition temperature. When a temperature above the glass transition temperature, but below the melting temperature, has been reached, the current is removed slowly enough to allow the material to cool and crystallize into a low resistance state ('write 1' current region, FIG. 2). The device can be returned to an amorphous state by allowing more current through the device, thus heating the material above the melting temperature, and then quickly removing the current to quench the material into an amorphous, high resistance state ('write 0' current region, FIG. 2).

Chalcogenide materials, those containing S, Se, or Te, have been the most widely investigated materials for electronic resistance variable memory applications since the discovery of the electronic resistance switching effect in a chalcogenide material ( $\text{As}_{30}\text{Te}_{48}\text{Si}_{12}\text{Ge}_{10}$ ) by Ovshinsky almost 40 years ago [see Ovshinsky, S. R. "Reversible Electrical Switching

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Phenomena in Disordered Structures" *Phys. Rev. Lett.* 21 (1968), 1450-1453]. Chalcogenide materials are desirable for use in electronic memories due to the wide range of glasses they can form and the corresponding wide variety of glass transition and melting temperatures. One of the most well studied resistance switching chalcogenide materials is the  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  (GST) alloy [see Bez, R.; Pirovano, A. "Non-volatile memory technologies: emerging concepts and new materials" *Materials Science in Semiconductor Processing* 7 (2004) 349-355; and Hudgens, S.; Johnson, B. "Overview of Phase-Change Chalcogenide Nonvolatile memory Technology" *MRS Bulletin*, November 2004, 829-832]. GST has been used successfully in phase-change memory arrays [see Storey, T.; Hunt, K. K.; Graziano, M.; Li, B.; Bumgarner, A.; Rodgers, J.; Burcin, L. "Characterization of the 4 Mb Chalcogenide-Random Access Memory" *IEEE Non-Volatile Memory Technology Symposium* (2005) 97-104; and Cho, W. Y.; Cho, B.-H.; Choi, B.-G.; Oh, H.-R.; Kang, S.; Kim, K.-S.; Kim, K.-H.; Kim, E.-E.; Kwak, C.-K.; Byun, H.-G.; Hwang, Y.; Ahn, S.; Koh, G.-H.; Jeong, G.; Jeong, H.; Kim, K. "A 0.18-um 3.0-V 64-Mb nonvolatile phase-transition random access memory (PRAM)" *IEEE J Solid-State Circuits* 40 (2005) 293-300] but there have been many challenges to the implementation of a phase-change memory product such as the high programming current requirements, variation in switching voltages and ON/OFF resistance ratios, thermal stresses on the materials, and their adhesion to the electrodes. See also U.S. Patent Publication 2007/0029537 A1.

## SUMMARY OF THE INVENTION

Our work has focused on exploring alternative materials and device structures suitable for phase-change memory operation. Recently we have investigated devices consisting of two chalcogenide layers (FIG. 3) instead of a single layer alloy of chalcogenide material (such as GST). By using two chalcogenide layers, one a Ge-chalcogenide (the memory layer), and the other a Sn-chalcogenide (the metal chalcogenide layer), we hoped to reduce the voltages, currents, and switching speeds needed for phase-change memory operation without the need for a complicated physical device structure [see Cho, W. Y.; Cho, B.-H.; Choi, B.-G.; Oh, H.-R.; Kang, S.; Kim, K.-S.; Kim, K.-H.; Kim, E.-E.; Kwak, C.-K.; Byun, H.-G.; Hwang, Y.; Ahn, S.; Koh, G.-H.; Jeong, G.; Jeong, H.; Kim, K. "A 0.18-um 3.0-V 64-Mb nonvolatile phase-transition random access memory (PRAM)" *IEEE J Solid-State Circuits* 40 (2005) 293-300; Lankhorst, M. H. R.; Ketelaars, Bas W. S. M. M.; Wolters, R. A. M. "Low-cost and nanoscale non-volatile memory concept for future silicon chips" *Nature Materials* 4 (2005) 347-352; and Hamann, H. F.; O'Boyle, M.; Martin, Y. C.; Rooks, M.; Wickramasinghe, H. K. "Ultra-high-density phase-change storage and memory" *Nature Materials* 5 (2006) 383-387].

Devices with three types of material stacks were fabricated for this study:  $\text{GeTe/SnTe}$ ;  $\text{Ge}_2\text{Se}_3/\text{SnTe}$ ; and  $\text{Ge}_2\text{Se}_3/\text{SnSe}$ . While Te-based chalcogenides are well studied for use in phase-change memory applications [see Bez, R.; Pirovano, A. "Non-volatile memory technologies: emerging concepts and new materials" *Materials Science in Semiconductor Processing* 7 (2004) 349-355; Lacaita, A. L. "Phase-change memories: state-of-the-art, challenges and perspectives" *Solid-State Electronics* 50 (2006) 24-31; and Chen, M.; Rubin, K. A.; Barton, R. W. "Compound materials for reversible, phase-change optical data storage" *Appl. Phys. Lett.* 49 (1986)



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502-504], we know of no reports of phase-change memory operation with GeSe-based binary glasses. In this work, we have explored the possibility of inducing a phase-change response in the  $\text{Ge}_2\text{Se}_3/\text{Sn}$  chalcogenide stack structures. We selected the  $\text{Ge}_2\text{Se}_3$  glass since, like the GeTe glass, it contains homopolar Ge—Ge bonds which we believe may provide nucleation sites for crystallization during the phase-change operation, thus improving the phase-change memory response [see An, S.-H.; Kim, D.; Kim, S. Y. “New crystallization kinetics of phase-change of  $\text{Ge}_2\text{S}_2\text{Te}_5$  at moderately elevated temperature” *Jpn. J. Appl. Phys.* 41 (2002) 7400-7401]. Additionally, the  $\text{Ge}_2\text{Se}_3$  glass offers the advantage of higher glass transition temperatures ( $\text{Ge}_2\text{Se}_3$ :  $T_g > 613$  K [see Feltz, A. *Amorphous Inorganic Materials and Glasses*, VCH Publishers Inc., New York, 1993, pg. 234]) over the Te-based glasses (GeTe:  $T_g = 423$  K [see Chen, M.; Rubin, K. A. “Progress of erasable phase-change materials” *SPIE Vol. 1078 Optical Data Storage Topical Meeting* (1989) 150-156]; GST:  $T_g = 473$  K [see Hamann, H. F.; O’Boyle, M.; Martin, Y. C.; Rooks, M.; Wickramasinghe, H. K. “Ultra-high-density phase-change storage and memory” *Nature Materials* 5 (2006) 383-387]), thus providing more temperature tolerance during manufacturing.

One possible benefit of the metal-chalcogenide layer is the potential for formation of an Ohmic contact between the electrode and the memory layer due to the presence of a low bandgap material like SnTe ( $E_g = 0.18$  eV at 300K [see Esaki, L.; Stiles, P. J. “New Type of Negative Resistance in Barrier Tunneling” *Phys. Rev. Lett.* 16 (1966) 1108-1111]) between the electrode and the chalcogenide switching layer. An Ohmic contact will allow a lower voltage to be applied to the memory cell since a Schottky barrier does not need to be overcome in order to achieve the current necessary for phase-change switching. Another potential benefit of the Sn-chalcogenide layer is better adhesion of the memory layer to the electrode. The better adhesion provided by the SnTe layer may help prevent delamination of the electrode from the chalcogenide memory layer, as can occur after repeated thermal cycles [see Hudgens, S.; Johnson, B. “Overview of Phase-Change Chalcogenide Nonvolatile memory Technology” *MRS Bulletin*, November 2004, 829-832]. In addition to these potential benefits, the Sn-chalcogenide may provide a region with ‘graded’ chalcogenide concentration between the Sn-chalcogenide and the Ge-chalcogenide memory switching layer due to the ability of the chalcogenide to form bridging bonds between the Sn and Ge atoms in the Sn-chalcogenide and Ge-chalcogenide layers, respectively. Lastly, as we show in this work, the Sn-chalcogenide material may assist in phase-change memory switching by donating Sn-ions to the Ge-chalcogenide layer during operation, thus allowing chalcogenide materials which normally do not exhibit phase change memory switching to be chemically altered post processing into an alloy capable of phase change response.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a graph depicting an example distribution of low and high resistance values defining a logic ‘1’ and ‘0’ state, respectively, of a resistance variable memory.

FIG. 2 is a graph depicting the relationship between current through the memory cell material and the formation of a low (write ‘1’) or high (write ‘0’) resistance state.

FIG. 3 is a top perspective schematic view of the device structures according to the present invention as tested. The notation Ge-Ch/Sn-Ch indicates a device with this structure with the films listed in the order nearest the bottom electrode to nearest the top electrode.

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FIG. 4 is a graph depicting XRD spectra of SnTe and SnSe evaporated films.

FIG. 5 is a TEM image of a GeTe/SnTe device according to the present invention.

FIG. 6 is a set of IV-curves for three unique GeTe/SnTe devices according to the present invention, showing the device-to-device variation typically observed in these devices. A positive potential was applied to the top electrode in each case.

FIG. 7 is a representative IV-curve for a GeTe/SnTe device according to the present invention, with a negative potential applied to the top electrode. A positive potential has never been applied to the device top electrode prior to this measurement.

FIG. 8 is a representative IV-curve for a  $\text{Ge}_2\text{Se}_3/\text{SnTe}$  device according to the present invention, with a positive potential applied to the top electrode.

FIG. 9 is a representative IV-curve for a  $\text{Ge}_2\text{Se}_3/\text{SnTe}$  device according to the present invention, with a negative potential applied to the top electrode. A positive potential has never been applied to the device top electrode prior to this measurement.

FIG. 10 is a representative IV-curve for a  $\text{Ge}_2\text{Se}_3/\text{SnSe}$  device according to the present invention, with a positive potential applied to the top electrode.

FIG. 11 is an IV-curve of a  $\text{Ge}_2\text{Se}_3/\text{SnSe}$  device according to the present invention, with the top electrode at a negative potential. A positive potential has never been applied to the device top electrode prior to this measurement.

FIG. 12 is an IV-curve of a  $\text{Ge}_2\text{Se}_3/\text{SnSe}$  device according to the present invention, obtained with a negative potential applied to the top electrode after the application of a positive potential ‘conditioning’ signal consisting of a DC current sweep limited to 30 nA.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to the Figures, there are shown some, but not the only, embodiments of the invention.

FIG. 3 shows a top perspective view of a device structure, according to the present invention, used in this study. The device structure consists of a via through a nitride layer to a W bottom electrode deposited on 200 mm p-type Si wafers. The chalcogenide material layers were deposited with the Ge-chalcogenide layer first, followed by the Sn-chalcogenide layer. Prior to deposition of the first chalcogenide layer, the wafers received an  $\text{Ar}_+$  sputter etch to remove residual material and any oxide layer that may have formed on the W electrode. The  $\text{Ge}_2\text{Se}_3$  layer was deposited by sputtering with an Ulvac ZX-1000 from a target composed of pressed  $\text{Ge}_2\text{Se}_3$  powder. The GeTe, SnTe, and SnSe layers were prepared by thermal evaporation of GeTe, SnTe, and SnSe (all from Alfa Aesar, 99.999% purity) using a CHA Industries SE-600-RAP thermal evaporator equipped with three 200 mm wafer planetary rotation. The rate of material deposition was monitored using an Inficon IC 6000 with a single crystal sensor head. The base system pressure was  $1 \times 10^{-7}$  Torr prior to evaporation.

Using the planetary rotator, evaporated films were deposited on two types of wafers simultaneously in each experiment: (1) a film characterization wafer consisting of a p-type Si wafer substrate with the layers  $350 \text{ \AA}$  W/ $800 \text{ \AA}$   $\text{Si}_3\text{N}_4$  and, (2) two wafers processed for device fabrication consisting of vias etched through a  $\text{Si}_3\text{N}_4$  layer to a W electrode for bottom electrode contact (FIG. 3). The film characterization wafer present in each evaporation step was used to characterize the

actual thin-film material stoichiometry post evaporation since thermally evaporated films often have a stoichiometry different than the starting material. The evaporation chamber was opened to the ambient atmosphere between the GeTe, SnTe, and SnSe film depositions in order to expose the GeTe films to similar ambient atmospheric conditions as the sputtered  $\text{Ge}_2\text{Se}_3$  films which had to get exposed to the atmosphere during transfer from the sputtering tool to the evaporator for the Sn-chalcogenide film deposition. After the evaporation step(s) were complete, the device fabrication wafers continued processing through top electrode deposition (350 Å sputtered W), photo steps, and dry etch to form fully functional devices consisting of a bottom electrode, chalcogenide material layers, and top electrode. Dry etch was performed by ion-milling with a Veeco ion-mill containing a quadrupole mass spectrometer for end-point detection.

The films were characterized with ICP to determine the variation in composition of the film compared to the starting material. ICP data provided film stoichiometry with an accuracy of  $\pm 0.8\%$  using a Varian Vista-PRO radial ICP. The chalcogenide films were removed from the wafer prior to ICP analysis with an etching solution of 1:1 HCl:HNO<sub>3</sub>. XRD, performed with a Siemens DS5000, was used to qualitatively identify amorphous or polycrystalline films. TEM measurements were made with a Phillips Model CM300.

Electrical measurements were made using a Micromanipulator 6200 microprobe station equipped with temperature controllable wafer chuck, a Hewlett-Packard 4145B Parameter Analyzer, and Micromanipulator probes with W tips (Micromanipulator size 7A). The tested devices were 0.25 μm in diameter with 80 μm×80 μm pads for electrical contact to the top and bottom electrodes.

## Results and Discussion

The GeTe and  $\text{Ge}_2\text{Se}_3$  films were amorphous as deposited with no observable XRD peaks. The SnTe and SnSe films were polycrystalline, as indicated by their XRD spectra (FIG. 4). Due to the nature of the evaporation process, and the relatively high pressure of the evaporation chamber prior to film deposition (1E-7 Torr), oxygen is most likely incorporated into the SnTe, SnSe, and GeTe films during deposition. Our previous X-ray photoelectron spectroscopy measurements on evaporated films have shown that the percentage of oxygen in an evaporated film can be as high as 10%.

Table 1 provides the ICP results for the film characterization wafers that were included in the evaporation step with the device wafers in this study, as well as for a sputtered  $\text{Ge}_2\text{Se}_3$  film wafer. Note that the only elements measured by ICP analysis were Ge, Se, Sn, and Te. The presence of oxygen is not detected with ICP and is not factored into the overall film composition. The evaporated SnTe and SnSe layers are almost stoichiometric, whereas the GeTe layer was deposited slightly Te-rich (53% compared to 50%). The sputtered  $\text{Ge}_2\text{Se}_3$  films are stoichiometric.

TABLE 1

Device types fabricated for this study and their actual thin film compositions measured with ICP (within $\pm 0.8\%$ ). Note that ICP analysis does not measure oxygen in the film, therefore the concentrations of the elements indicate only relative concentrations of Ge, Se, Sn, or Te in the film.		
Device Stack	Layer 1 Composition	Layer 2 Composition
GeTe/SnTe	$\text{Ge}_{47}\text{Te}_{53}$	$\text{Sn}_{49}\text{Te}_{51}$
$\text{Ge}_2\text{Se}_3/\text{SnTe}$	$\text{Ge}_{40}\text{Se}_{60}$	$\text{Sn}_{49}\text{Te}_{51}$
$\text{Ge}_2\text{Se}_3/\text{SnSe}$	$\text{Ge}_{40}\text{Se}_{60}$	$\text{Sn}_{49}\text{Se}_{51}$

(a) GeTe/SnTe device—A TEM cross section image of a GeTe/SnTe device is shown in FIG. 5. The evaporated material has reduced step coverage over the sidewalls of the via, leading to thinner films in this region of the devices. The pre-sputter etch clean etches into the W bottom electrode by roughly 300 Å. Thus, the device structure consists of not only a via through  $\text{Si}_3\text{N}_4$ , but also an indented bottom electrode which subsequently allows the chalcogenide phase-change material to be in contact at the sides and bottom of the layer near the metal electrode.

Typical DC IV-curves for devices with the GeTe/SnTe stack structure are shown in FIG. 6. These curves were collected by forcing the current thru the devices from 10 pA to 100 nA and measuring the corresponding voltage across the devices with the positive potential on the electrode adjacent to the SnTe layer (the top electrode). The IV-curves, showing a ‘snap-back’, i.e. negative resistance, at the threshold voltage as well as a reduction in device resistance after sweeping the current, are characteristic of a phase-change memory device. There is slight device-to-device variation observed in IV-curves of unique devices (FIG. 6a-c). However, in each case the threshold voltage is less than 1.8 V and there are at least two ‘snap-back’ regions in the IV-curves. The additional ‘snap-back’ responses indicate that our devices may exhibit multi-state behavior. However, the stability of each resistance state is as yet unclear. Additionally, the cycling endurance and switching properties of each state have not been explored. Similar results, though not as well defined as those in FIG. 6, have been obtained on stacked Chalcogenide layers of GST/Si-doped GST [see Lai, Y. F.; Feng, J.; Qiao, B. W.; Cai, Y. F.; Lin, Y. Y.; Tang, T. A.; Cai, B. C.; Chen, B. “Stacked chalcogenide layers used as multi-state storage medium for phase-change memory” *Appl. Phys. A* 84 (2006) 21-25] and are being explored as multi-state phase-change memories.

When the electrodes are reversed and a negative potential is placed on the device top electrode, the DC IV-curve is altered, as shown in FIG. 7, but the device still exhibits phase-change behavior. In this electrical configuration the threshold voltage has increased above 2V. In either potential polarity configuration, the threshold voltage and programming currents that we observe for the GeTe/SnTe stack structure are lower than those reported for recent single devices comprised of GST [see Lv, H.; Zhou, P.; Lin, Y.; Tang, T.; Qiao, B.; Lai, Y.; Feng, J.; Cai, B.; Chen, B. “Electronic Properties of GST for Non-Volatile Memory” *Microelectronics Journal*, in press].

Table 2 provides a comparison of the typical initial resistance of a device prior to switching and the programmed resistance after switching, as well as the measured threshold voltage for both the positive and negative current sweep cases. The resistances were measured at +20 mV in each case, a potential too low to perturb the state of the bit. Included in Table 2 are the typical programmed resistances when the current is swept to 1 mA (for both the positive and negative potential cases). Of note is the programmed resistance when

the current is swept to a  $-1$  mA (top electrode at a negative potential) compared to the case when the current is swept to  $+1$  mA. There is almost an order of magnitude decrease in the programmed resistance when  $+1$  mA is forced at the top electrode compared to the bottom electrode. However, our results indicate that it is not necessary to use a current as high as  $1$  mA in order to program the bits (see the  $100$  uA results in Table 2).

TABLE 2

Typical initial and programmed resistances and threshold voltages for devices programmed with $\pm 100$ uA and $\pm 1$ mA of current. A '—' indicates no measurable response. Resistance was measured at $20$ mV.				
Device Stack	Initial Resistance (Ohms)	Programmed Resistance (Ohms) $\pm 100$ uA/ $\pm 100$ uA	Programmed Resistance (Ohms) $\pm 1$ mA/ $\pm 1$ mA	Threshold Voltage $\pm$ sweep/ $\pm$ sweep
GeTe/SnTe	$>5 \times 10^6$	$1 \times 10^4/2 \times 10^4$	$5 \times 10^2/3 \times 10^3$	$1.6$ V/ $2.5$ V
Ge <sub>2</sub> Se <sub>3</sub> /SnTe	$>6 \times 10^6$	$2 \times 10^3/3 \times 10^5$	$7 \times 10^2/7 \times 10^2$	$3.7$ V/ $3.7$ V
Ge <sub>2</sub> Se <sub>3</sub> /SnSe	$>6 \times 10^6$	$1 \times 10^3/—$	$5 \times 10^2/—$	$3.7$ V/ $—$
Ge <sub>2</sub> Se <sub>3</sub> /SnSe (low current test)	$>6 \times 10^6$	$2 \times 10^8$ ( $+30$ nA limit)/ $1 \times 10^5$ ( $-2$ uA limit)	No data	$—/2.5$ V

(b) Ge<sub>2</sub>Se<sub>3</sub>/SnTe device—When the GeTe glass is replaced with a Ge<sub>2</sub>Se<sub>3</sub> glass, the resultant Ge<sub>2</sub>Se<sub>3</sub>/SnTe devices exhibit resistance variable memory switching, FIG. 8. However, there are two distinct differences in the DC IV-curve compared to the GeTe/SnTe case. First, the threshold voltage, when the top electrode is at a positive potential, is higher in the Ge<sub>2</sub>Se<sub>3</sub> case (greater than  $3.5$  V compared to less than  $1.8$  V for the GeTe/SnTe case). Second, the threshold voltage occurs at a current which is an order of magnitude lower than in the GeTe devices. Additionally, the Ge<sub>2</sub>Se<sub>3</sub>/SnTe devices exhibit better device-to-device consistency in their IV-curves than the evaporated GeTe/SnTe devices, most likely due to the better via sidewall film step-coverage inherent in the sputtered Ge<sub>2</sub>Se<sub>3</sub> film, as well as a reduction in film impurities (such as oxygen).

FIG. 9 shows the corresponding current sweep IV-curves for the Ge<sub>2</sub>Se<sub>3</sub>/SnTe structure with a negative potential on the top electrode. The IV-curves for this negative current sweep show a much less well-defined threshold voltage than the positive current sweep case. In addition, the current at the threshold voltage is much higher than the positive current sweep case (FIG. 8). However, the negative potential Ge<sub>2</sub>Se<sub>3</sub>/SnTe IV-curve (FIG. 9) shows similar threshold voltages and currents to the negative potential GeTe/SnTe IV-curve (FIG. 7).

(c) Ge<sub>2</sub>Se<sub>3</sub>/SnSe device—When the SnTe layer is replaced with a SnSe layer in the Ge<sub>2</sub>Se<sub>3</sub> stack, resistance switching is observed (FIG. 10) when a positive voltage is applied to the top electrode. The DC IV-curves for the Ge<sub>2</sub>Se<sub>3</sub>/SnSe device (FIG. 10) and the Ge<sub>2</sub>Se<sub>3</sub>/SnTe device (FIG. 8) show no differences due to the SnSe layer. However, when a negative potential is applied to a device that has not previously seen a positive potential, no threshold voltage is observed in the IV-curve (FIG. 11). This is in contrast to the case of the negative potential applied to a Ge<sub>2</sub>Se<sub>3</sub>/SnTe device (FIG. 9) where phasechange switching is observed with a threshold voltage less than  $3$  V.

The absence of a threshold voltage in the negative current sweep IV-curve (FIG. 11), but its presence in the positive current sweep IV-curve (FIG. 10) of the Ge<sub>2</sub>Se<sub>3</sub>/SnSe device implies that during the application of a positive potential there may be Sn-ion migration from the SnSe layer into the Ge<sub>2</sub>Se<sub>3</sub> layer which chemically alters the Ge<sub>2</sub>Se<sub>3</sub> layer to a (Ge<sub>2</sub>Se<sub>3</sub>)<sub>x</sub>Sn<sub>y</sub> alloy capable of phase-change operation.

Te<sup>2-</sup>-ions from the SnTe layer may be electrically driven by the negative potential into the underlying Ge<sub>2</sub>Se<sub>3</sub> glass layer, thus creating (Ge<sub>2</sub>Se<sub>3</sub>)<sub>x</sub>Te<sub>y</sub> regions capable of phase-change switching.

Te<sup>2-</sup>-ions from the SnTe layer may be electrically driven by the negative potential into the underlying Ge<sub>2</sub>Se<sub>3</sub> glass layer, thus creating (Ge<sub>2</sub>Se<sub>3</sub>)<sub>x</sub>Te<sub>y</sub> regions capable of phase-change switching.

To explore the possibility that the phase-change switching in the Ge<sub>2</sub>Se<sub>3</sub>/SnSe device is facilitated by Sn-ion migration into the Ge<sub>2</sub>Se<sub>3</sub> layer, the Ge<sub>2</sub>Se<sub>3</sub>/SnSe device, was initially tested by applying a positive potential 'conditioning' signal to the top electrode. This 'conditioning' signal was a DC current sweep limited to  $30$  nA in order to prevent any phase-change from occurring, but with enough potential ( $\sim 3$  V) to drive Sn-ions into the Ge<sub>2</sub>Se<sub>3</sub> layer. After this 'conditioning' signal was applied to the Ge<sub>2</sub>Se<sub>3</sub>/SnSe device, a negative potential was applied to the top electrode and the IV curve was measured (FIG. 12). A voltage 'snap-back' is observable at two separate current values,  $60$  nA and  $100$  nA. This double 'snap-back' is representative of the IV curves of the devices measured with this conditioning technique. Device resistances after application of the negative potential (post conditioning) were in the range of  $30$  kOhms to  $200$  kOhms.

The Ge<sub>2</sub>Se<sub>3</sub>/SnTe and GeTe/SnTe stacks were also subjected to this 'conditioning' signal test. However, their negative current DC IV-curves were not appreciably altered after application of the positive 'conditioning' voltage.

## Conclusions

Phase-change memory switching was observed in devices consisting of two stacked layers of chalcogenide material: a Ge-based layer (GeTe or Ge<sub>2</sub>Se<sub>3</sub>), and a tin chalcogenide layer (SnTe or SnSe). The observed switching is dependent upon the polarity of potential applied to the electrode adjacent to the SnTe or SnSe layer. When a positive potential is applied to this electrode, the formation of Sn-ions and their migration into the adjacent GeTe or Ge<sub>2</sub>Se<sub>3</sub> layer most likely contributes to the phase-change response of the material.

We attribute the switching of the Ge<sub>2</sub>Se<sub>3</sub>/SnTe device under negative applied potential, with no previously applied positive 'conditioning' voltage, to the migration of Te anions into the Ge<sub>2</sub>Se<sub>3</sub> layer during application of the negative potential. The possible Te anion migration may alter the Ge<sub>2</sub>Se<sub>3</sub> glass layer into a (Ge<sub>2</sub>Se<sub>3</sub>)<sub>x</sub>Te<sub>y</sub> alloy capable of phase-change memory operation.

In the case of the  $\text{Ge}_2\text{Se}_3/\text{SnSe}$  device, no Te anions are available to migrate into the  $\text{Ge}_2\text{Se}_3$  glass layer when a negative potential is applied to the top electrode, and no phase-change behavior is observed in the IV-curve. If it were possible for Se anions to be forced into the  $\text{Ge}_2\text{Se}_3$  glass from the SnSe layer (analogous to the Te anions from the SnTe layer), they would succeed only in making the  $\text{Ge}_2\text{Se}_3$  glass Se-rich and thus still incapable of phase-change switching. Alternatively, if a positive potential is initially applied across the  $\text{Ge}_2\text{Se}_3/\text{SnSe}$  device and the current is limited to a low enough value to prohibit Joule heating, but still allow a high enough potential across the device for Sn-ion migration, Sn-ions may migrate into the  $\text{Ge}_2\text{Se}_3$  layer, creating a  $(\text{Ge}_2\text{Se}_3)_x\text{Sn}_y$  alloy which is capable of phase-change switching when a negative potential is applied to the top electrode.

The addition of metal ions, forced into the chalcogenide switching layer during the first 'forming' electrical pulse, not only facilitates electrical switching, but it also may allow for more than one ON resistance state. This phase change memory alloy, formed in-situ, may exhibit more than one crystallization temperature. Each crystallization temperature corresponds to a unique phase of the material, and thus a unique resistance. This means that by proper selection of the metal that is allowed to migrate into the chalcogenide glass, the alloy can be tuned to have more than one crystalline phase.

We further investigated this concept by synthesizing materials using the  $\text{Ge}_x\text{Se}_y$  chalcogenide glass and adding small concentrations (1 and 3%) of various metals, and measuring the thermal properties of these materials. Metals we have tested include, Sn, Zn, In, and Sb. The Sn and In addition showed the presence of two crystallization regions whereas the Zn showed three crystallizations regions. Thus the  $\text{Ge}_x\text{Se}_y\text{Zn}_z$  alloy has the potential to have four logic states. This alloy can be formed in-situ, for example, by using a device comprising the layers of  $\text{Ge}_2\text{Se}_3/\text{ZnSe}$ .

GeTeSn materials have been well studied for their application as optical phasechange materials [see Chen, M.; Rubin, K. A. "Progress of erasable phase-change materials" *SPIE Vol. 1078 Optical Data Storage Topical Meeting* (1989) 150-156]. GeTe exhibits fast crystallization under optically induced phasechange operation (<30 ns) and it crystallizes in a single phase (no phase separation) making it attractive for phase-change operation. However, the number of optically induced write/erase cycles that could be achieved was quite low (<500) [see Chen, M.; Rubin, K. A. "Progress of erasable phase-change materials" *SPIE Vol. 1078 Optical Data Storage Topical Meeting* (1989) 150-156]. Our initial electrical cycling endurance tests on the GeTe/SnTe and  $\text{Ge}_2\text{Se}_3/\text{SnTe}$  devices and have shown endurance greater than 2 million cycles. Due to the potential for parasitic capacitances during the endurance cycling measurements, care must be taken in the measurement experimental setup [see Ielmini, D.; Mantegazza, D.; Lacaita, A. L. "Parasitic reset in the programming transient of PCMs" *IEEE Electron Device Letters* 26 (2005) 799-801]; with this in mind, better cycling measurements are currently in progress [see Campbell, K. A.; Anderson, C. M., *Microelectronics Journal* 38 (2007) 52-59].

Future studies will investigate the temperature dependence, AC switching and lifetime cycling endurance of each of these device types. Additionally, we will investigate the phase-change switching response of stack structure devices that use a metal-chalcogenide layer with a metal different than tin, such as zinc, which is expected to have much different mobility in an applied field as well as a much different chemical incorporation into the Ge-chalcogenide glass layer. It is possible that the presence of Ge—Ge bonds in the Ge-based layer assist in the incorporation of the metal ions or of

the Te anions into the glass by providing an energetically feasible pathway (that of the Ge—Ge bonds) for Te- or metal-ion incorporation [see Narayanan, R. A.; Asokan, S.; Kumar, A. "Influence of Chemical Disorder on Electrical Switching in Chalcogenide Glasses" *Phys. Rev. B* 63 (2001) 092203-1-092203-4; and Asokan, S. "Electrical switching in chalcogenide glasses—some newer insights" *J Optoelectronics and Advanced Materials* 3 (2001) 753-756]. Ge—Ge bonds are known to be thermodynamically unstable [see Feltz, A. *Amorphous Inorganic Materials and Glasses*, VCH Publishers Inc., New York, 1993, pg. 234], and in the presence of other ions, will easily break and allow formation of a new bond (e.g. GeTe or GeSn). Future work will investigate the role of the Ge—Ge bond by testing the electrical performance of devices made with Ge-chalcogenide stoichiometries that provide no Ge—Ge bonds, such as  $\text{Ge}_{2.5}\text{Se}_{7.5}$ .

Although this invention has been described above with reference to particular means, materials, and embodiments, it is to be understood that the invention is not limited to these disclosed particulars, but extends instead to all equivalents within the scope of the following claims.

I claim:

1. A device suitable for phase change memory operation comprising:
  - a first layer comprising a chalcogenide material;
  - a second layer comprising a metal chalcogenide material; wherein application of an electric field across the device causes a metal ion to move from the second layer to the first layer wherein the first layer incorporates the metal and forms a new chalcogenide alloy with a plurality of crystalline phases.
2. The device of claim 1 wherein the metal is either Sn, Zn, In, or Sb.
3. The device of claim 1 which comprises three or more logic states.
4. The device of claim 1 comprising a stack of chalcogenide-containing layers which exhibit phase change switching only after a reverse polarity voltage potential is applied across the stack causing ion movement into an adjacent layer and thus "activating" the device to act as a phase change random access memory device or a reconfigurable electronics device when the applied voltage potential is returned to the normal polarity.
5. The device of claim 1, wherein the first layer comprises a Ge-chalcogenide material.
6. The device of claim 5, wherein first layer comprises GeTe.
7. The device of claim 5, wherein first layer comprises  $\text{Ge}_2\text{Se}_3$ .
8. The device of claim 1, wherein the second layer comprises a Sn-chalcogenide material.
9. The device of claim 8, wherein second layer comprises SnTe.
10. The device of claim 8, wherein second layer comprises ZnSe.
11. The device of claim 8, wherein second layer comprises ZnSe.
12. The device of claim 1, wherein the device is fabricated on a p-type Si wafer.
13. The device of claim 1, further comprising a third layer upon which the second layer is fabricated.
14. The device of claim 13, wherein the third layer comprises  $\text{Si}_3\text{N}_4$ .
15. The device of claim 1, further comprising a top electrode fabricated over the first layer and a bottom electrode fabricated under the second layer.

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**16.** The device of claim **15**, wherein the bottom electrode comprises tungsten.

**17.** The device of claim **15**, wherein the top electrode comprises tungsten.

**18.** The device of claim **15**, wherein the second layer is 5  
connected to the bottom electrode with a via.

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**19.** The device of claim **1**, wherein the second layer comprises Zn, In, or Sb.

**20.** The device of claim **1**, wherein the new chalcogen alloy comprises Ge, Se, and Zn.

\* \* \* \* \*